**FIGURE 1.2** (a) First transistor (Property of AT&T Archives. Reprinted with permission of AT&T.) and (b) first integrated circuit (Courtesy of Texas Instruments.)
FIGURE 1.7 Silicon lattice and dopant atoms
FIGURE 1.8
p-n junction diode
structure and symbol
FIGURE 1.10  Transistor symbols and switch-level models
FIGURE 1.9 nMOS transistor (a) and pMOS transistor (b)
FIGURE 1.3  (a) Intel 1101 SRAM (© IEEE 1967 [Vadasz69]) and (b) 4004 microprocessor (Reprinted with permission of Intel Corporation.)
FIGURE 1.4 Transistors in Intel microprocessors [Intel10]
FIGURE 1.5 Clock frequencies of Intel microprocessors
FIGURE 1.6 Process generations. Future predictions from [SIA2007].
FIGURE 1.1 Size of worldwide semiconductor market (Courtesy of Semiconductor Industry Association.)
(a) CMOS Inverter

(a) CMOS Inverter
\( Y = \overline{A} \cdot \overline{B} \)
FIGURE 1.74 2-input NAND gate stick diagram
Figure 1.75 Level-sensitive latch stick diagram
FIGURE 1.62  MIPS floorplan

- mips (4.8 M\lambda^2)
- control 2550\lambda \times 380\lambda (1.0 M\lambda^2)
- datapath 2550\lambda \times 1320\lambda (3.4 M\lambda^2)

wiring channel: 25 tracks = 200\lambda

height determined from PLA size width matches datapath

width determined from slice plan

10 I/O pads

5000 \lambda

3500 \lambda

1900 \lambda

2550 \lambda

3500 \lambda

5000 \lambda
**FIGURE 1.64** MIPS controller layout (synthesized)
FIGURE 1.63  MIPS layout
FIGURE 1.65 Synthesized MIPS processor
FIGURE 1.67 MIPS datapath layout
FIGURE 1.69 PLA for control FSM
**FIGURE 1.71** Engineer holding processed 12-inch wafer. Photograph courtesy of the Intel Corporation.
FIGURE 1.72 MIPS processor photomicrograph (only part of pad frame shown)
**FIGURE 1.73** Chip in a 40-pin dual-inline package